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## REMARKS/ARGUMENTS

Claims 1 - 23 have been cancelled and replaced by new claims 24 - 44. Claims 24 - 44 are the claims pending in the application. It will noted that these new claims are in European format and that they are patterned on the claims that are on file in the corresponding European application.

## Traversal of the prior art rejections

The rejection of claims 1 - 23 under 35 U.S.C. 102(b) as being anticipated by Passint et al (US 6,101,181) (hereinafter Passint) is respectfully traversed. The Passint patent deals with multiprocessor computer systems having up to hundreds of thousands of processing elements or nodes and referred to as massively parallel processing (MPP) systems. In a typical multiprocessor MPP system, every processing element can directly address all of memory, including the memory of another (remote) processing element, without involving the processor at that processing element. Instead of treating processing element-to-remote-memory communications as an I/O operation, reads or writes to another processing element's memory are accomplished in the same manner as reads or writes to the local memory. (Col. 1, lines 25-37, BACKGROUND OF THE INVENTION.)

The Passint reference deals with:

Multiprocessor computer systems having up to hundreds or thousands of processing element nodes are typically referred to as massively parallel processing (MPP) systems. In a typical multiprocessor MPP system, every

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processing element can directly address all of memory, including the memory of another (remote) processing element, without involving the processor at that processing element. (Passint, first paragraph under "Background of the Invention," emphasis added).

The disclosure deals with torus topology which is a ring formed in each dimension and can transfer from one node to all of the nodes in the same dimension and back to the original node. (Passint, paragraph bridging cols. 1 and 2.) In the "Summary of the Invention," Passint points out that:

Each processing element node has at least one processor and memory. Physical communication links interconnect the processing element nodes in a n-dimensional topology. Routers route messages between the plurality of processing element nodes on the physical communication links. Each router includes input ports for receiving messages, output ports for sending messages from the router, two types of virtual channels, a lookup table associated with the input port having a lookup table virtual channel number, and a virtual channel assignment mechanism. Each type of virtual channel has virtual channel buffers assigned to each physical communication link and is capable of storing messages communicated between the processing element nodes over the physical communication links. The virtual channel assignment mechanism assigns an output next virtual channel number for determining the type of virtual channel to be used for routing from a next router along a given route. The next virtual channel number is assigned based on the lookup table virtual channel number and an input next virtual channel number received from a previously router along the given route. (Passint, first paragraph in the "Summary of the Invention", col. 3, lines 47-67.)

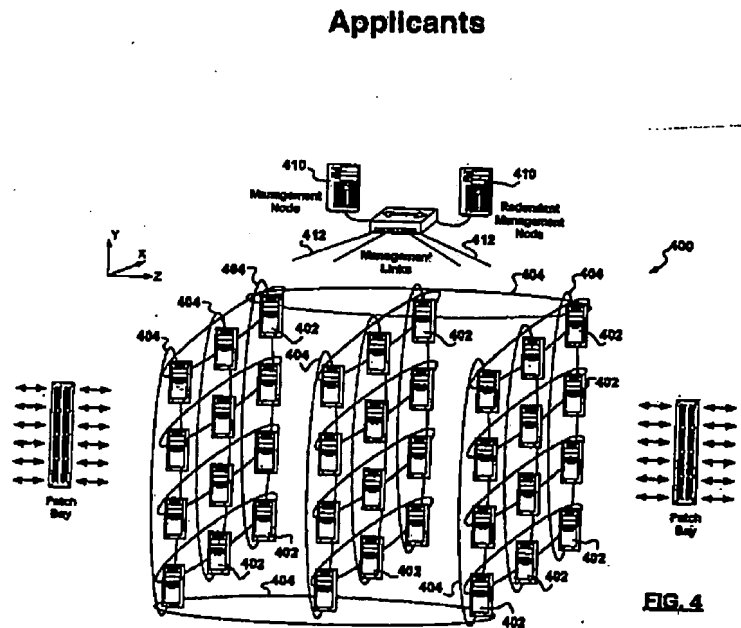
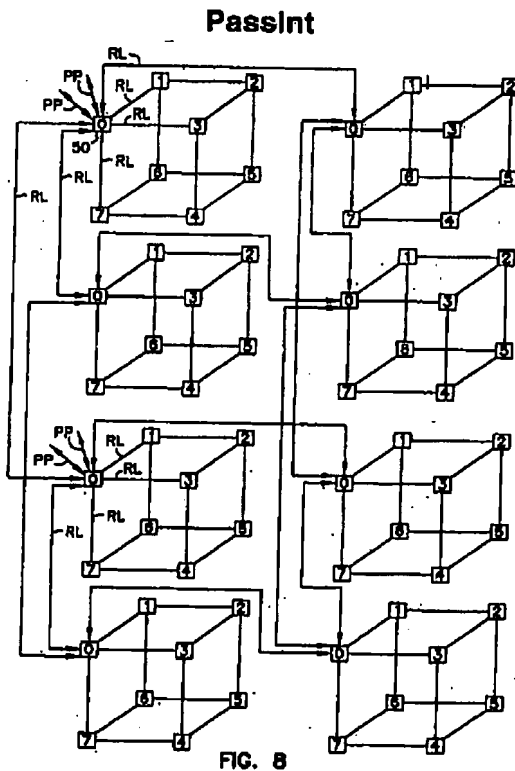
Fig. 8 of Passint referred to by the Examiner is described in col. 8 as the following:

An example six dimensional (6D) hypercube topology multiprocessor system is modeled in Fig. 8. In Fig. 8, 64 router chips 50 are employed. There are two processor ports from each router, such as those labeled PP from router 0, to couple each router to two nodes to create a double bristled topology. Thus the doubled bristled 6D

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topology produces a 128 node multiprocessor system having 256 processors in a two processor per node system or 512 processors in a four processor per node system. The router links, such as those labeled RL from node 0 form the 6D hypercube topology. For clarity, only the node 0 links in the fourth, fifth, and sixth dimensions are shown in Fig. 7.

Fig. 8 of Passint is shown side-by-side of applicants' Fig. 4 as follows:



In contrast, applicants' Fig. 4 is an exemplary embodiment showing the individual clustered nodes 402 arranged in x, y and z slices with each router cluster node 402 physically connected via 404 to adjacent router cluster nodes 402 in the x, y and z

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directions. Only the two z-toroidal interconnections are shown in order to improve clarity. However, every router cluster node 402 participates in a z-toroid of which there are twelve in total. The toroidal interconnections 404 implement a dedicated cluster intra-connection network. This is reflected in applicants' claim 24 in the following:

...a plurality of external links for enabling said cluster-based router to exchange traffic with a plurality of nodes of said packet-switched communication network; each cluster node of said N cluster nodes (402) being adapted to operate as a core router cluster node and as an edge router cluster node;

the internal links (404) connect said cluster nodes in an intra-connection network adapted to provide a high path diversity for a plurality of packet processing flows routed over said intra-connection network between edge router nodes; and

the cluster nodes connected to external links are adapted to operate as edge router cluster nodes,

whereby a specified routing capacity is obtained for said cluster-based router by selecting N and selecting a configuration of said intra-connection network.

This is not disclosed or suggested by the art.

New method claim 39 reads:

...i) selecting a number N and a configuration for said cluster-based router for obtaining a specified routing capacity and port count for said cluster-based router,

ii) connecting N cluster nodes (402) via internal links in an intra-connection network according to said configuration;

iii) connecting a selected number of cluster nodes designated to operate as edge router cluster nodes over a plurality of external links for enabling connection of said cluster-based router in a communication network; and

iv) routing packets along packet processing flows established between two edge router cluster node over a plurality of core router cluster nodes.

This is likewise not disclosed or suggested in the Passint art.

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In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

*Jim Zegeer*

Jim Zegeer, Reg. No. 18,957  
Attorney for Applicants

Suite 108  
801 North Pitt Street  
Alexandria, VA 22314

Telephone: 703-684-8333

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In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.

**CERTIFICATE OF TRANSMISSION/MAILING**

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature: *Jim Zegeer*  
Jim Zegeer

Date: Aug 7 2007